

## 5W-30-520-10-M0X, 30 – 520 MHz, 5 Watt, Tunable Filter

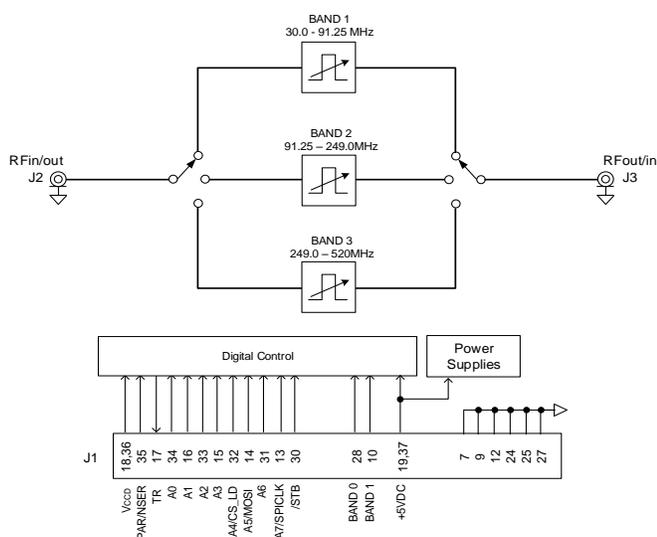
### Typical Applications

- UAVs
- Applications where small size, high power, and high performance are required
- Military Radios
- Military Radar
- SATCOM
- Test and Measurement Equipment
- Industrial and Medical Equipment

### Features

- Typical features are listed below but are not exhaustive
- 37 dBm CW continuous in-band power handling
- 40 dBm CW continuous out-of-band power handling<sup>1</sup>
- 47 dBm IIP3 typical
- 25  $\mu$ s typical tune time
- 18 dBc typical selectivity at  $f_c \pm 10\%$
- 2.5 dB typical insertion loss

### Functional Diagram



### Description

The new **ERF-5W™** filter takes Pole/Zero's® MINI-ERF technology to a higher level of RF power handling, with 5W (average) in-band power handling, and covering the entire military tactical radio tuning range of 30 to 520 MHz in one integrated package. This tuning range is accomplished by the use of three poles of selectivity and multiple internal tunable filters along with high performance RF band select switches. The tunable filters are designed to minimize size and power consumption, while maintaining high RF power handling and linearity characteristics. Interface (SPI)-based bus. **ERF-5W™** filters are available in both single and dual-channel configurations.



<sup>1</sup> Out of band RF power handling refers to signals that are at least twenty percent (20%) removed from the tuned center frequency and is frequency dependent: 5W signals applied between 30 and 75 MHz, 8W from 75 to 175 MHz, and 10 W from 175 to 520 MHz.

## 1.0 Ordering Information

Table 1. Ordering Options

Series	Frequency Range (MHz)	% Bandwidth (3 dB)	Package	Series Options
5W	30-520	10	M01	Single Filter
D5W	30-520	10	M02	Dual Filter

Note: Options may be limited to particular frequency bands and/or configurations. Consult Pole/Zero for your application.

Example product number: Product # 5W-30-520-10-M01

## 2.0 Block Diagram

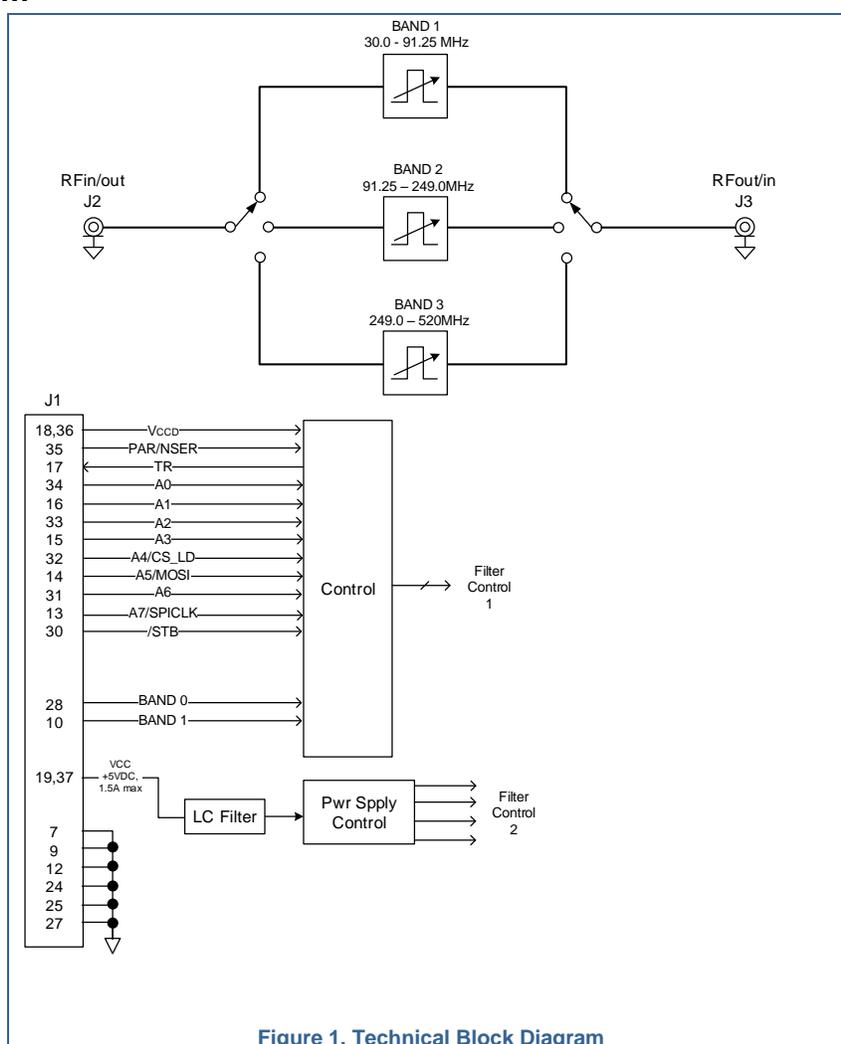
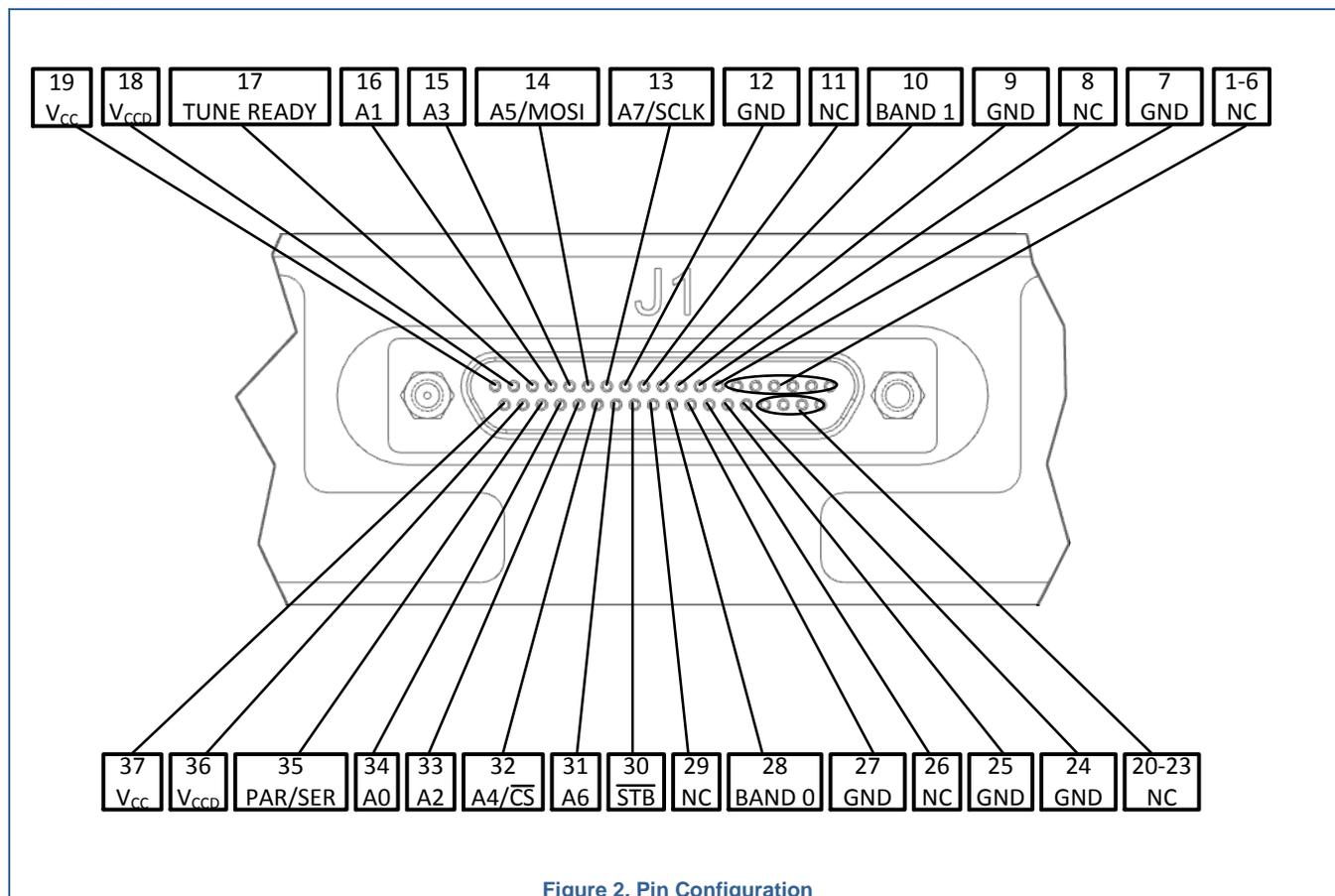


Figure 1. Technical Block Diagram

### 3.0 Pinout and Functional Information

#### 3.1 Pinout



### 3.2 Pin Description

Table 2. Pin Functions and Descriptions

Pin Number	Label	Description
1-6, 8, 20-23, 26, 29	N/C	No Connect – Factory use only pins. Shorting or connecting these pins may affect the performance and functionality of the filter. Leave these pins floating.
7, 9, 12, 24, 25, 27	GND	Digital Ground
11	FACTORY	This is an internal factory calibration pin and it must be pulled to $V_{CCD}$ through a 10 k $\Omega$ pull-up resistor or connected to GND in order to avoid damage to the 5W-ERF.
10	BAND 1	Band Select Bit 1 <sup>2</sup> - The most significant bit of the band selection for the parallel interface.
13	A7	Parallel Tune Offset Bit 7 (MSB) – In Parallel interface mode, data is latched on the falling edge of $\overline{STB}$ and indicates which frequency the filter should tune to (A7 = MSb, A0 = LSb).
	SCLK	Serial Tune Clock – In serial mode, SCLK is used to clock in the tune data. Data is latched on the rising edge of SCLK.
14	A5	Parallel Tune Offset Bit 5
	MOSI	Serial Tune Interface Master Output Slave Input – Data is applied to MOSI for transferring a tune command to the device in serial mode. Each bit of data is latched on the rising edge of SCLK. The filter accepts serial tune command lengths of 16-bits.
15	A3	Parallel Tune Offset Bit 3 <sup>2</sup>
16	A1	Parallel Tune Offset Bit 1 <sup>2</sup>
17	TUNE READY	Tune Ready Indicator – This pin normally remains low. When $\overline{CS}$ or $\overline{STB}$ is taken low to initiate a tune in either SPI or Parallel tune modes, the TUNE READY pin transitions high to indicate the filter is processing the tune command. After the command has been completely processed, the TUNE READY pin will transition back low indicating that the tune process is finished and that the filter is ready for a new tune command.
18, 36	$V_{CCD}$	Digital Interface Supply Input – Used to set the digital interface logic voltage level between 1.65 V and 5 V. If using 5 V logic to control the 5W-ERF, $V_{CCD}$ should be +5 V, if using 3.3 V logic to control the 5W-ERF, $V_{CCD}$ should be +3.3 V, etc.
19, 37	$V_{CC}$	+5V Power Supply Input +/- 10%
28	BAND 0	Band Select Bit 0 - The least significant bit of the band selection for the parallel interface.
30	$\overline{STB}$	Parallel Strobe – In parallel mode, when $\overline{STB}$ is taken low, the control circuitry wakes up and data is latched on BAND1, BAND0, and A7-A0. It is important to keep $\overline{STB}$ held low until the data is completely latched. When the control circuitry finishes waking up, the filter is commanded to the frequency latched on the parallel data interface. (This pin is pulled to $V_{CCD}$ internally via a 3.01 k $\Omega$ resistor)
31	A6	Parallel Tune Offset Bit 6 <sup>2</sup>
32	A4	Parallel Tune Offset Bit 4 <sup>2</sup>
	$\overline{CS}$	SPI Chip Select
33	A2	Parallel Tune Offset Bit 2 <sup>2</sup>
34	A0	Parallel Tune Offset Bit 0 <sup>2</sup> – The least significant bit of the frequency offset for parallel mode.
35	$\overline{PAR/SER}$	Parallel/Serial Mode Selection – Leaving $\overline{PAR/SER}$ pulled to +3.3 V will enable the parallel tune command interface. Keeping $\overline{PAR/SER}$ floating or pulled to GND will enable the SPI (serial) tune command interface. A power cycle is required to change modes. (This pin is internally pulled to GND with a 3.01 k $\Omega$ resistor.)

<sup>2</sup> When the filter is set for Serial Control, the following unused input pins must be connected to GND (or alternately pulled high to  $V_{CCD}$  with 10 k $\Omega$  resistor): Pin 15 (A3), Pin 16 (A1), Pin 31 (A6), Pin 33 (A2), Pin 34 (A0), pin 11 (Factory programming only), pin 10 (BAND\_1), and pin 28 (BAND\_0). **Failure to do this could damage the unit.**

## 4.0 Specifications

### 4.1 Absolute Maximum Ratings<sup>3</sup>

Voltages are referenced to GND (ground = 0V). Operating at room temperature (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	-	-0.3	6.5	V
$V_{CCD}$	Digital supply voltage	-	-0.5	6.5	V
$V_I$	Input voltage	On all digital interface input pins	-0.5	6.5	V
$I_K$	Digital interface pin input clamp current	$V_I < 0$	-50	-	mA
$I_{OK}$	Digital interface pin output clamp current	$V_O < 0$	-50	-	mA
$P_{INBAND}$	In-band RF input power level	Signal is in passband $f_0 = 30 - 520 \text{ MHz}$	-	37	dBm
$P_{OUTBAND}$	Out-of-band RF input power level	-	-	40 <sup>1</sup>	dBm
$T_{RATE}$	Maximum tune rate (frequency hopping)	-	-	1	kHz

### 4.2 Handling Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$T_S$	Storage temperature	-	-65	150	°C

### 4.3 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
$V_{CC}$	Supply voltage	-	4.5	5.0	5.5	V
$V_{CCD}$	Digital supply voltage	-	1.65	-	5.5	V
$P_{IN}$	Maximum RF input power for linear operation	Signal is in passband	-	-	37	dBm
$T_A$	Ambient temperature	-	-40	-	+85	°C

### 4.4 Electrical Characteristics

All specifications at  $T_A = 23 \text{ °C}$ ,  $V_{CC} = 5.0 \text{ V}$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
$I_{CC\_STATIC}$	$V_{CC}$ current consumption, statically tuned	At nominal $V_{CC}$ voltage	0.270	-	1.5	A
$I_{CC\_HOP}$	$V_{CC}$ current consumption, hopping	Nominal $V_{CC}$ , hopping at 1 kHz	0.270	-	2.0	A
$V_{IH}$	Digital high level input voltage	On all digital interface input pins except PAR/SER	$0.75 * V_{CCD}$	-	-	V
		On PAR/SER	2.3	-	-	
$V_{IL}$	Digital low level input voltage	On all digital interface output pins except PAR/SER	-	-	$0.2 * V_{CCD}$	V
		On PAR/SER	-	-	0.66	

<sup>3</sup> Maximum operating conditions before damage occurs.

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
$I_{IH}/I_{IL}$	Digital Interface pin input logic current	-	-100	-	+100	$\mu$ A
$F_{RANGE}$	Tunable frequency range	-	30	-	520	MHz
$Z_O$	Input/output impedance	-	-	50	-	$\Omega$
RL	Return loss	$Z_o = 50 \Omega$	12.0	15	-	dB
IL	Insertion loss	-	-	2.5	3.5	dB
BW	Bandwidth (3 dB)	-	7.4	10.0	11.6	%
SEL <sub>10%</sub>	Selectivity 10% removed from the center frequency	$f_o \pm 10\%$	14	18	-	dBc
SEL <sub>20%</sub>	Selectivity 20% removed from the center frequency	$f_o \pm 20\%$	30	35	-	dBc
SEL <sub>ULTIMATE</sub>	Selectivity at $2x f_o$					
	30 to 91.25 MHz	$2 \times f_o$	-	65	50	dBc
	91.25 to 249 MHz	$2 \times f_o$	-	65	50	dBc
	249 to 520 MHz	$2 \times f_o$	-	50	30	dBc
IIP3	Input third order intermodulation intercept point	2 tone, In-Band	+44	+47	-	dBm
NF	Noise figure	-	-	TBD	TBD	dB
$T_{TUNE}$	Tune time	-	-	25	50	$\mu$ s
$F_{DRIFT}$	Center frequency drift over temperature	-40°C to +85°C	-	-50	-80	ppm/°C

### 4.5 Typical Characteristics

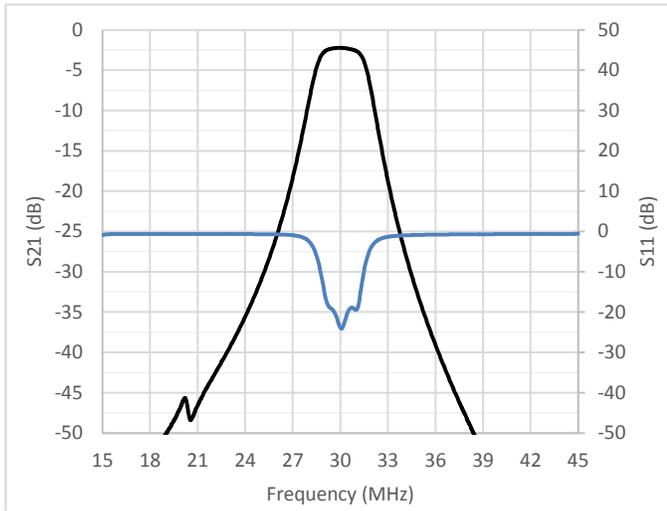


Figure 3. Filter response at 30 MHz

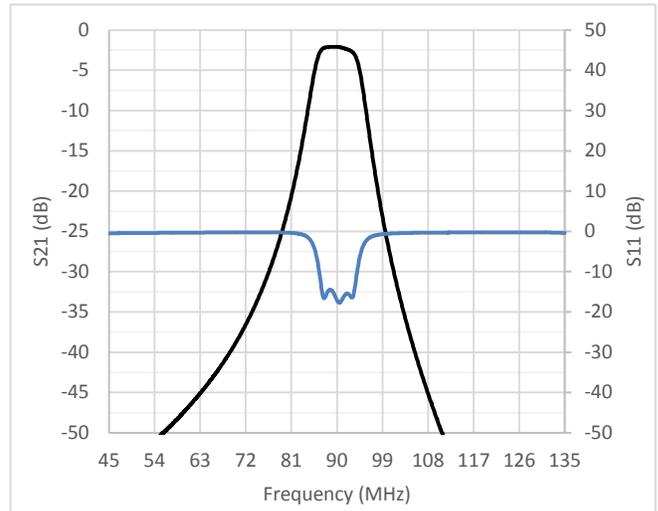


Figure 4. Filter Response at 90 MHz

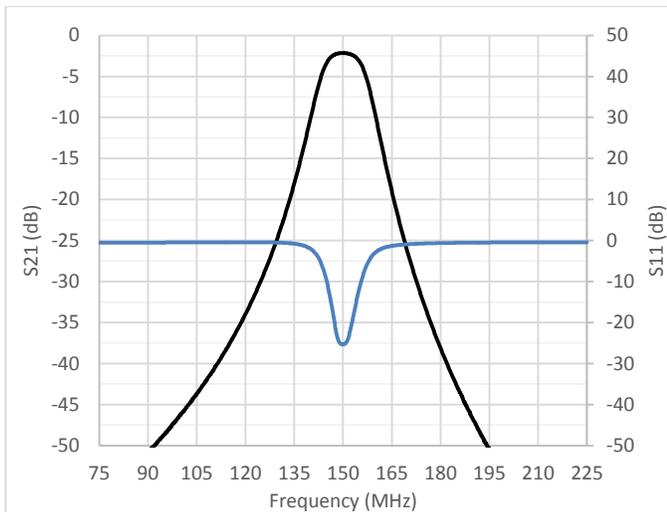


Figure 5. Filter Response at 150 MHz

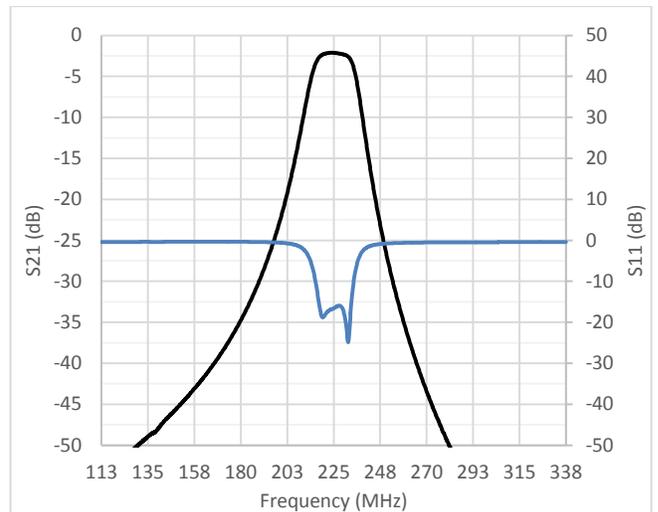


Figure 6. Filter Response at 225 MHz

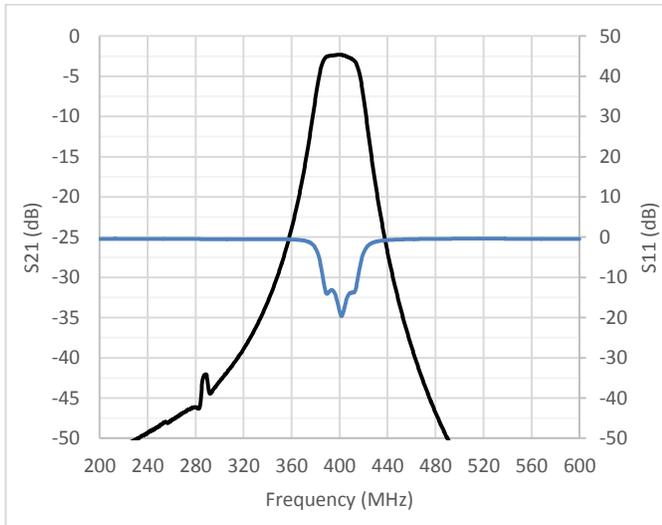


Figure 7. Filter Response at 400 MHz

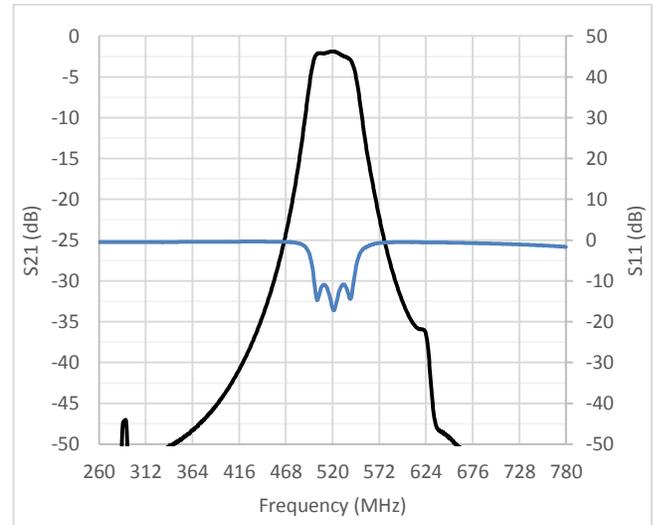


Figure 8. Filter Response at 520 MHz

## 4.6 Timing Requirements

### 4.6.1 SPI Interface Timing

The SPI tune interface is a standard SPI interface with Mode = 0 (CPOL = 0, CPHA = 0). There are always 16 data bits loaded for the tune command. Any bits that do not affect the frequency offset of the filter should always be set to 0. The interface receives the data most significant byte and most significant bit first.

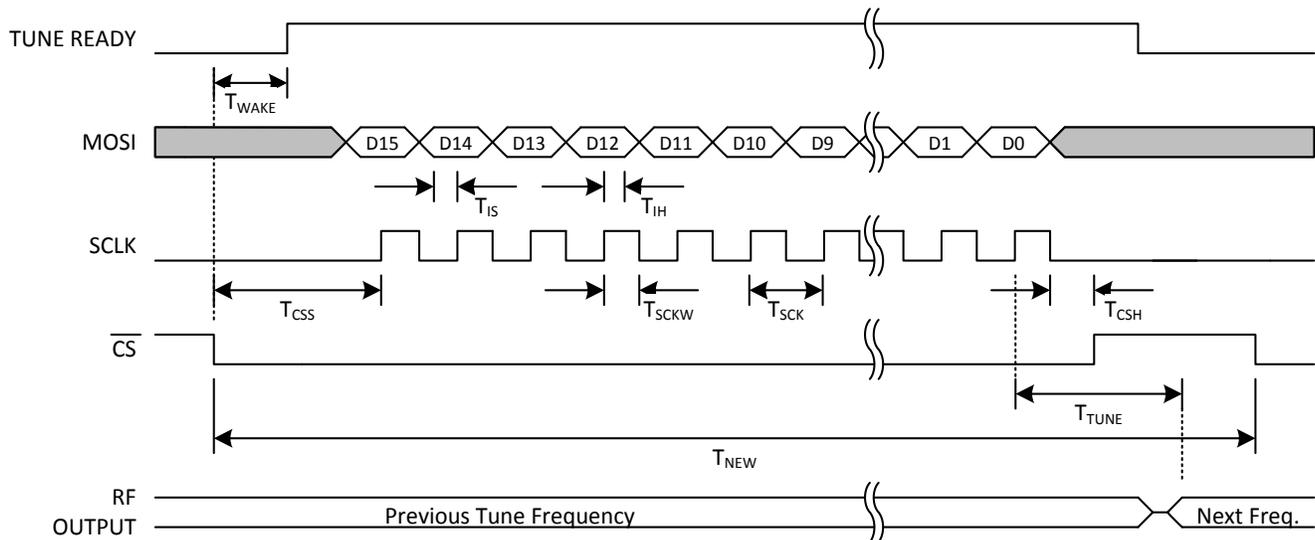


Figure 9. Serial Timing Diagram

Table 3. SPI Timing Characteristics

$V_{CC} = +5.0\text{ V} \pm 5\%$ ,  $V_{CCD} = +5.0\text{ V} \pm 5\%$ ,  $GND = 0\text{ V}$

Parameter	Parameter	Min.	Max.	Unit
$T_{WAKE}$	Wakeup Time – The amount of time from $\overline{CS}$ transitioning low until TUNE READY transitions high.	-	7	$\mu\text{s}$
$T_{CSS}$	$\overline{CS}$ Setup Time – The amount of time needed from when $\overline{CS}$ transitions low until the first rising edge of SCLK.	100	-	ns
$T_{IS}$	MOSI Setup – The amount of time data needs to be present on MOSI before the rising edge of SCLK.	31.25	-	ns
$T_{IH}$	MOSI Hold – The amount of time data needs to be held on MOSI after the rising edge of SCLK.	31.25	-	ns
$T_{SCK}$	SCLK Period	62.5	-	ns
$T_{SCKW}$	SCLK Duty Cycle	$\frac{T_{SCLK}}{2}$	-	ns
$T_{SCLKF}/$ $T_{SCLKR}$	SCLK Rise/Fall Time (not shown)	0	10	ns/V
$T_{CSH}$	$\overline{CS}$ Hold Time – The amount of time $\overline{CS}$ needs to remain low after the last falling edge of SCLK.	100	-	ns
$T_{NEW}$	New Command Delay – The amount of between falling edges of $\overline{CS}$ . This is the time between the start of new tune commands.	1	-	ms
$T_{TUNE}$	Time from the last rising edge of clock until the RF response reaches 90%.	-	50	$\mu\text{s}$

#### 4.6.2 Parallel Interface Timing

The parallel tune command interface is a 10-bit wide synchronous parallel interface. Band 1 is the most significant band bit and Band 0 is the least significant band bit. A7 is the most significant tune offset bit and A0 is the least significant tune offset bit. Keeping  $\overline{\text{PAR/SER}}$  pulled to +3.3 V will enable the parallel tune command interface.

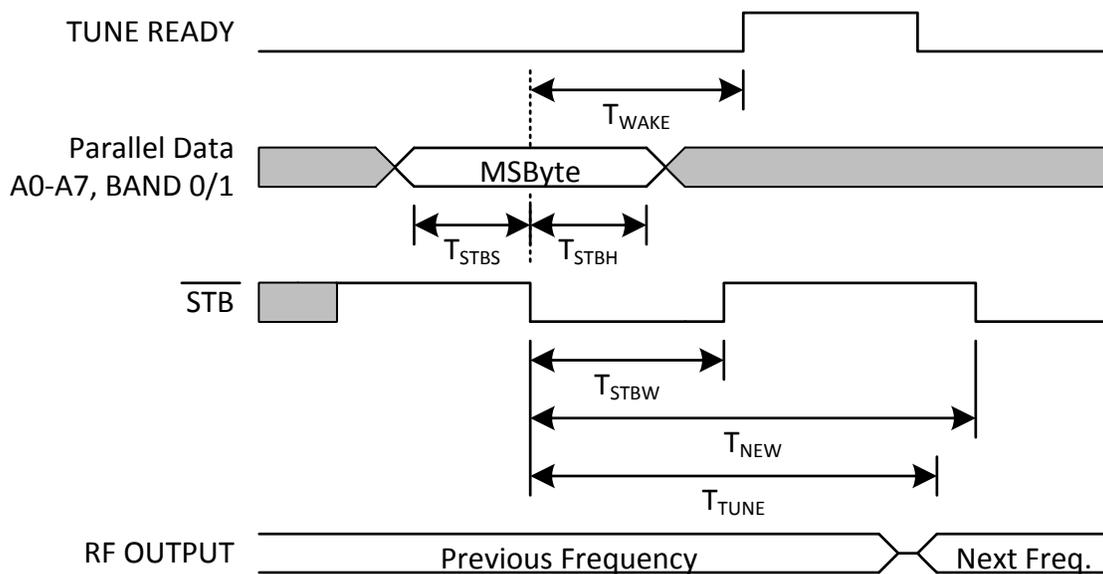


Figure 7. Parallel Timing Diagram

Table 4. Parallel Timing Characteristics

$V_{CC} = +5.0 \text{ V} \pm 5\%$ ,  $V_{CCD} = +5.0 \text{ V} \pm 5\%$ ,  $GND = 0 \text{ V}$

Symbol	Parameter	Min.	Max.	Unit
$T_{WAKE}$	Wakeup Time – The amount of time from $\overline{\text{STB}}$ transitioning low until TUNE READY transitions high.	-	7	$\mu\text{s}$
$T_{STBS}$	$\overline{\text{STB}}$ Setup Time – The amount of time needed from when parallel data is valid until $\overline{\text{STB}}$ transitions low.	100	-	ns
$T_{STBH}$	$\overline{\text{STB}}$ Hold Time – The amount of time needed to hold the parallel data after $\overline{\text{STB}}$ transitions low.	100	-	ns
$T_{STBW}$	$\overline{\text{STB}}$ Width – The amount needed to hold $\overline{\text{STB}}$ for the tune event to occur.	50	-	ns
$T_{NEW}$	New Command Delay – The amount of between falling edges of $\overline{\text{STB}}$ . This is the time between the start of new tune commands.	1	-	ms
$T_{TUNE}$	Time from the last rising edge of clock until the RF response reaches 90%.	-	50	$\mu\text{s}$

## 5.0 Functional Description

### 5.1 Tune Commands

In serial mode, the tune command is a two-byte tune word. The first byte (MSB) is the band the filter should tune to. The second byte (LSB) is the frequency offset in the chosen band. In parallel mode, the upper 6 bits from the MSB are discarded and the MSb of the band byte is loaded on the BAND 1 pin and the LSb of the band byte is loaded on the BAND 0 pin. The tune offset is loaded on the A7-A0 pins.

Table 5. Tune Command Properties

Symbol	Band	Value	Description
$f_{MIN}$	0	30.000 MHz	Minimum Tunable Frequency. $f_{MIN}$ is the absolute minimum frequency that the filter is capable of tuning to for the respective band.
	1	91.250 MHz	
	2	249.00 MHz	
$f_{MAX}$	0	91.250 MHz	Maximum Tunable Frequency. $f_{MAX}$ is the absolute maximum frequency that the filter is capable of tuning to. Sending tune commands greater than the maximum tunable frequency will result in an invalid tune condition. The frequency response of an invalid tune is unknown. Normal frequency response will return on the next valid tune command. Varies depending on the band.
	1	249.00 MHz	
	2	520.00 MHz	
$f_{STEP}$	0	0.245 MHz	Tune step size. $f_{STEP}$ is the minimum spacing between adjacent tune commands.
	1	0.631 MHz	
	2	1.084 MHz	
$f_{COM}$	All	$round\left(\frac{(f_{DESIRED} - f_{MIN})}{f_{STEP}}\right)$	Commanded Frequency. $f_{COM}$ is the commanded frequency that is sent over the SPI or parallel tune interface. The command can be calculated by subtracting $f_{MIN}$ from the desired frequency for the particular band, dividing the result by the $f_{STEP}$ of that band, and then rounding to the nearest integer command. The formula is used to select the closest possible frequency to the desired tune word. If the next lowest tune word is desired, replace the round operation with floor and if the next highest tune word is desired replace the round operation with ceil.

Table 6. Tune Command Format

Filter Model			Tune Word Format																
Part Series	$f_{MIN}$ (MHz)	$f_{MAX}$ (MHz)	(MSB)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	(LSB)
5W-30-520-10-M01	30	520	0	0	0	0	0	0	0	Band Bits		Commanded Frequency							
D5W-30-520-10-M02																			

## 6.0 Detailed Description

### 6.1 Digital Interface

Table 7. Band Bit Selection

Band Bits		Selected Band	Band Range (MHz)
For Serial Interface			
Bit 9	Bit 8		
For Parallel Interface			
BAND 1	BAND 0		
0	0	0	30.00 – 91.25
0	1	1	91.25 – 249.00
1	0	2	249.00 – 520.00
1	1	N/A	Unused

### 6.2 Example Tune Commands

Table 8. Example Tune Commands

$f_{DESIRED}$ (MHz)	Req. Band	Band (Hex)	$f_{MIN}$ of Band (MHz)	$f_{STEP}$ of Band (MHz)	$f_{COM}$ Calculation (Decimal)	$f_{COM}$ (Decimal)	$f_{COM}$ (Hex)	Tune Command (Hex)
30.0	0	0x00	30.0	0.245	$round\left(\frac{(30.0 - 30.0)}{0.245}\right)$	0	0x00	0x0000
66.92	0	0x00	30.0	0.245	$round\left(\frac{(66.92 - 30.0)}{0.245}\right)$	151	0x97	0x0097
91.25	0	0x00	30.0	0.245	$round\left(\frac{(91.25 - 30.0)}{0.245}\right)$	250	0xFA	0x00FA
91.25	1	0x01	91.25	0.631	$round\left(\frac{(91.25 - 91.25)}{0.631}\right)$	0	0x00	0x0100
147.8	1	0x01	91.25	0.631	$round\left(\frac{(147.8 - 91.25)}{0.631}\right)$	90	0x5A	0x015A
249.0	1	0x01	91.25	0.631	$round\left(\frac{(249.0 - 91.25)}{0.631}\right)$	250	0xFA	0x01FA
249.0	2	0x02	249.0	1.084	$round\left(\frac{(249.0 - 249.0)}{1.084}\right)$	0	0x00	0x0200
412.684	2	0x02	249.0	1.084	$round\left(\frac{(412.684 - 249.0)}{1.084}\right)$	151	0x97	0x0297
520.0	2	0x02	249.0	1.084	$round\left(\frac{(520.0 - 249.0)}{1.084}\right)$	250	0xFA	0x02FA

### 6.3 Additional Interface Detail

Table 9. Additional Pin Information

Pin Name	Description																												
BAND 1/BAND 0	<p>The BAND 1/BAND 0 pins define the band of the filter when tuning in parallel mode. The meaning of the pins is the same as bits 9 and 8 of the SPI tune command.</p> <p>BAND 1 = SPI command bit 9 BAND 0 = SPI command bit 8</p>																												
TUNE READY	<p>The TUNE READY indicator is a driven digital output. Do not connect any other push-pull output directly to this pin. The function of TUNE READY is to indicate the status of the digital interface during and after tune events. The normal logic state of the pin is low at power up. In this condition, the filter is waiting on a new tune command. The tune command can be applied without any delay since internal digital hardware latches the command immediately. When the internal control circuitry has finished fully waking up, the TUNE READY indicator is set high to indicate that the internal control circuitry is processing the tune command. When the internal control circuitry is finished processing the command and the filter has tuned to the commanded frequency, the TUNE READY indicator transitions low once again to notify the user that the filter is ready for a new tune command.</p>																												
$\overline{\text{STB}}$	<p>In parallel mode, <math>\overline{\text{STB}}</math> is transitioned low to latch the tune command into the filter and initiate the tune sequence. This pin is not used in SPI tune mode.</p>																												
PAR/ $\overline{\text{SER}}$	<p>The interface selection pin is used to select which digital control interface to use for sending tune commands. If the PAR/<math>\overline{\text{SER}}</math> pin is left open or pulled to ground (or below 0.66 V), the SPI (serial) tune mode will be selected. If the pin is pulled high (higher than 2.3) volts, the parallel tune mode will be selected. The input of this pin can swing as high as 5.5 volts to signify parallel tune mode without damage, but a 3.3 V input will consume less power.</p>																												
Unused Pins	<p>If the filter is used in SPI (serial) tune mode, the following pins will be unused. Please follow the proper connection procedure for the unconnected pins to ensure that damage is not caused to the filter:</p> <table border="1"> <thead> <tr> <th>Pin #</th> <th>Pin Function</th> <th>Unconnected Procedure</th> </tr> </thead> <tbody> <tr> <td>10</td> <td>BAND 1</td> <td rowspan="9">Connect to GND or alternatively pull high to <math>V_{\text{CCD}}</math> with a 10 k<math>\Omega</math> resistor.</td> </tr> <tr> <td>11</td> <td>NC</td> </tr> <tr> <td>15</td> <td>A3</td> </tr> <tr> <td>16</td> <td>A1</td> </tr> <tr> <td>28</td> <td>BAND 0</td> </tr> <tr> <td>30</td> <td><math>\overline{\text{STB}}</math></td> </tr> <tr> <td>31</td> <td>A6</td> </tr> <tr> <td>33</td> <td>A2</td> </tr> <tr> <td>34</td> <td>A0</td> </tr> </tbody> </table> <p>If the filter is used in parallel tune mode, the following pins will be unused. Please follow the proper connection procedure for the unconnected pins to ensure that damage is not caused to the filter:</p> <table border="1"> <thead> <tr> <th>Pin #</th> <th>Pin Function</th> <th>Unconnected Procedure</th> </tr> </thead> <tbody> <tr> <td>11</td> <td>NC</td> <td>Connect to GND or alternatively pull high to <math>V_{\text{CCD}}</math> with a 10 k<math>\Omega</math> resistor.</td> </tr> </tbody> </table>	Pin #	Pin Function	Unconnected Procedure	10	BAND 1	Connect to GND or alternatively pull high to $V_{\text{CCD}}$ with a 10 k $\Omega$ resistor.	11	NC	15	A3	16	A1	28	BAND 0	30	$\overline{\text{STB}}$	31	A6	33	A2	34	A0	Pin #	Pin Function	Unconnected Procedure	11	NC	Connect to GND or alternatively pull high to $V_{\text{CCD}}$ with a 10 k $\Omega$ resistor.
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11	NC	Connect to GND or alternatively pull high to $V_{\text{CCD}}$ with a 10 k $\Omega$ resistor.																											

## 7.0 Tune Time

Tune times include internal processing of the tune command data and the 90% settled RF amplitude response time of the filter. This time excludes the time required to load the tune command into the filter. Low level signal measurements were utilized to show the receive tune time that can be expected.

In addition, RF power in excess of +20 dBm is considered to be “hot switching” of the filter. While portions of the data taken in “Table 10. Typical RF Tune Times” was taken via “hot switching,” this does not imply that tuning operation of the filter into these levels can be done reliably. It is recommended that RF is less than +20 dBm during a tune event.

**Table 10. Typical RF Tune Times**

Freq. (MHz)		Band	Tune Time
From	To		RF Input Up to +37 dBm
30	91.25	VHFL (0)	16.0 us
91.25	30	VHFL (0)	17.1 us
91.25	249	VHFH (1)	15.4 us
249	91.25	VHFH (1)	16.6 us
249	520	UHF (2)	14.7 us
520	249	UHF (2)	16.2 us
30	520	VHFL (0) to UHF (2)	15.0 us
520	30	UHF (2) to VHFL (0)	16.9 us

## 8.0 Package Information

### 8.1 Package Detail

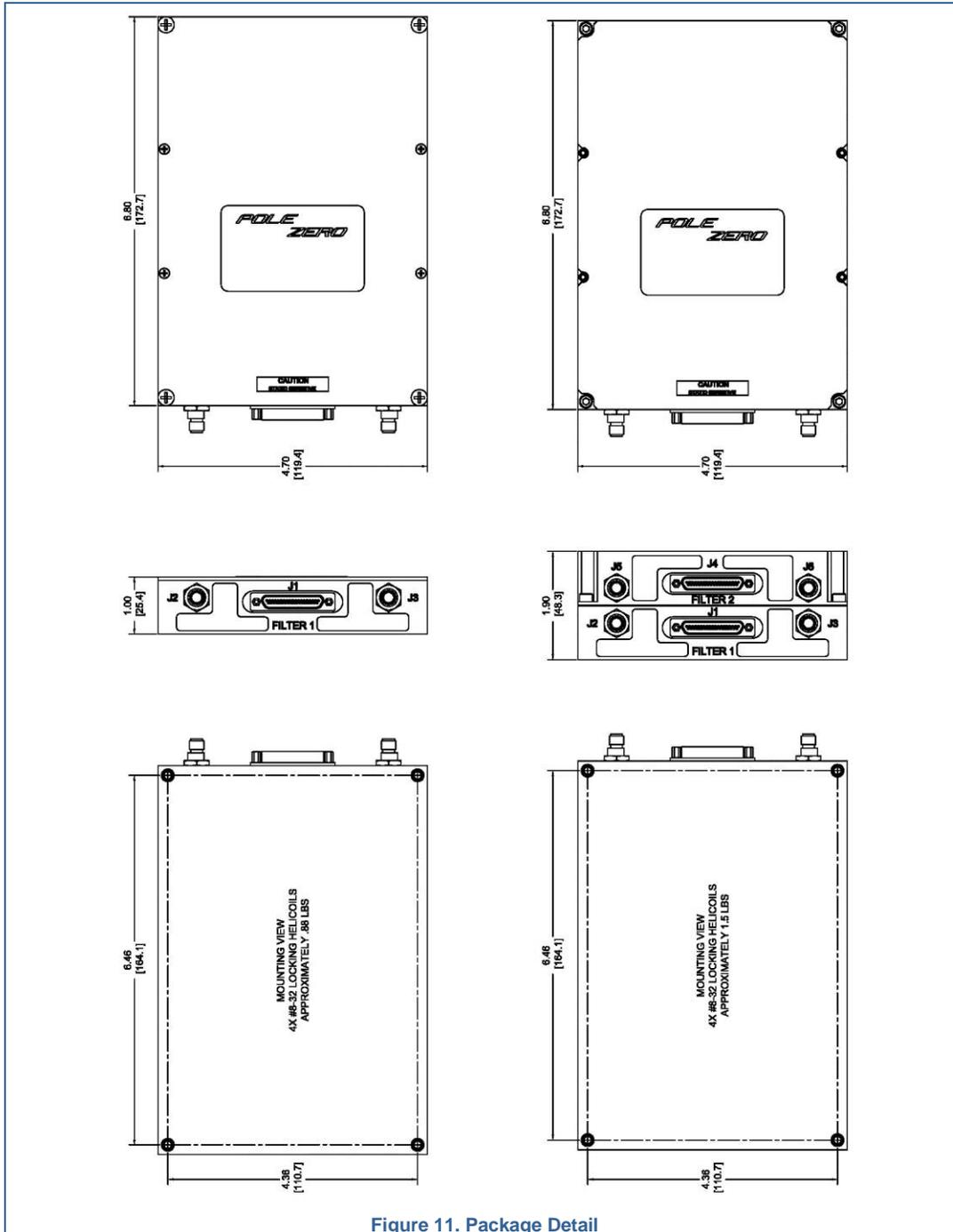


Figure 11. Package Detail

Configuration	Dimensions		Weight (Typical)	
	Inches	Millimeters	Ounces	Grams
Single	4.70 x 6.8 x 1.0	119.4 x 172.7 x 25.4	14.08	399
Dual	4.70 x 6.8 x 1.90	119.4 x 172.7 x 48.3	24.0	680

## 9.0 Application Information

### 9.1 Parallel Interface

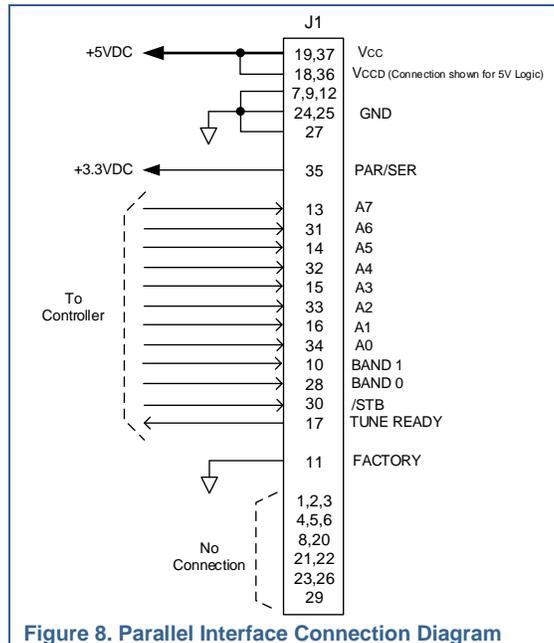


Figure 8. Parallel Interface Connection Diagram

### 9.2 Serial Interface (SPI)

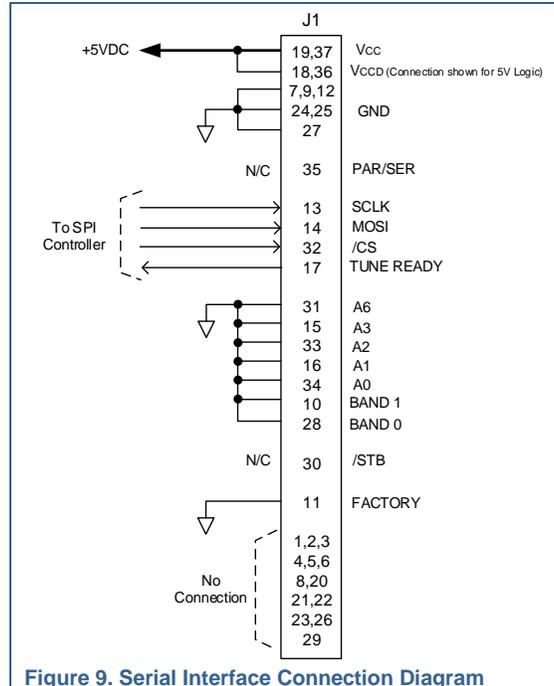


Figure 9. Serial Interface Connection Diagram

## 10.0 Safety Notes

### 10.1 Handling Information

#### Caution



This device contains electrostatic discharge sensitive devices and is sensitive to electrostatic discharge (ESD). Observe all precautions for handling electrostatic sensitive devices.

#### Caution



This device may produce potentially hazardous voltages. Take necessary precautions when handling this device while power is enabled.

#### Caution



This device is an MSD (moisture sensitivity device) level 4 component and should be packaged and handled according to the guidelines in J-STD-033.

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